

LINEAR INTEGRATED CIRCUITS

PREAMPLIFIER WITH ALC FOR CASSETTE RECORDERS

- EXCELLENT VERSATILITY in USE (V_s from 4 to 20V)
- HIGH OPEN LOOP GAIN
- LOW DISTORTION
- LOW NOISE
- LARGE AUTOMATIC LEVEL CONTROL RANGE
- GOOD SUPPLY RIPPLE REJECTION
- STEREO MATCHING BETTER THAN 3 dB

The TDA 1054M is a monolithic integrated circuit in a 16-lead dual in-line plastic package. The functions incorporated are:

- Low noise preamplifier
- Automatic level control system (ALC)
- High gain equalization amplifier
- Supply voltage rejection facility (SVRF).

It is intended as preamplifier in cassette tape recorders and players, dictaphones, compressor and expander in industrial equipments, Hi-Fi preamplifiers and in wire diffusion receivers; for stereo applications the ALC matching is better than 3 dB.

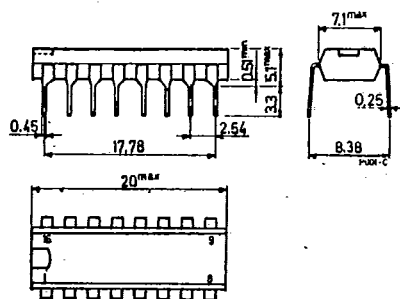
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
P_{tot}	Total power dissipation at $T_{amb} \leq 50^\circ\text{C}$	500	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

ORDERING NUMBERS: TDA 1054M mono applications
 2 TDA 1054M stereo applications

MECHANICAL DATA

Dimensions in mm



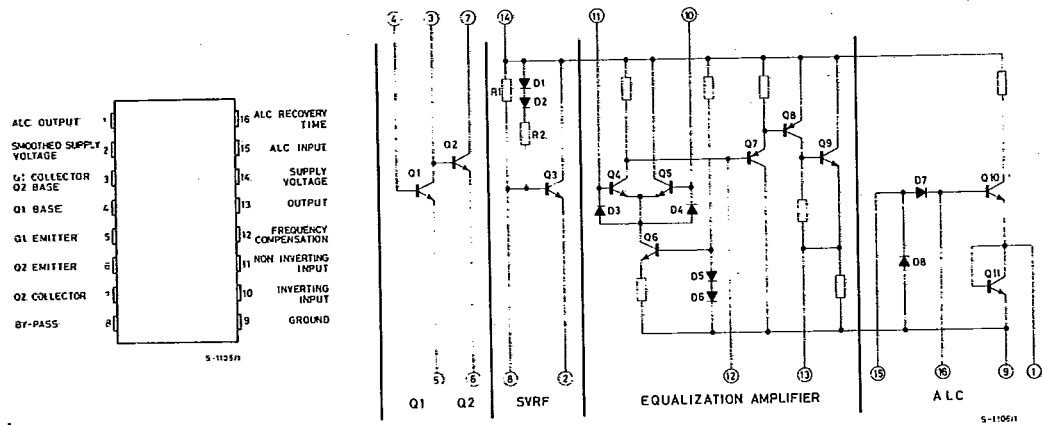
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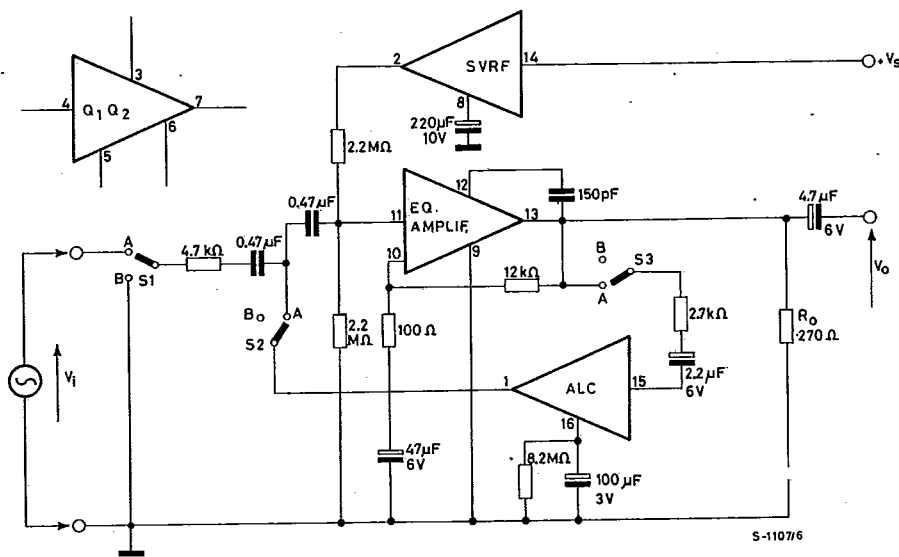
TDA1054M

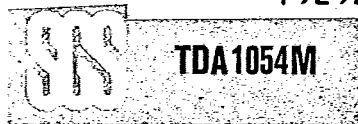
CONNECTION AND SCHEMATIC DIAGRAMS

(top view)



TEST CIRCUIT





THERMAL DATA

$R_{thJ-amb}$	Thermal resistance junction-ambient	max	200	°C/W
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ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, $T_{amb} = 25^{\circ}\text{C}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage	4		20	V
I_d	Quiescent drain current $V_s = 9\text{V}$ $R_L = \infty$ $S1 = S2 = S3 = B$		6		mA
h_{FE}	DC current gain $I_C = 0.1\text{ mA}$ $V_{CE} = 5\text{V}$	300	500		—
e_N	Input noise voltage (Q1) $I_C = 0.1\text{ mA}$ $V_{CE} = 5\text{V}$ $f = 1\text{ kHz}$		2		$\frac{nV}{\sqrt{Hz}}$
i_N	Input noise current (Q1)		0.5		$\frac{pA}{\sqrt{Hz}}$
NF	Noise figure (Q1) $I_C = 0.1\text{ mA}$ $V_{CE} = 5\text{ V}$ $R_g = 4.7\text{ k}\Omega$ $B (-3\text{ dB}) = 20\text{ to }10,000\text{ Hz}$		0.5	4	dB
G_V	Open loop voltage gain (for equalization amplifier) $V_s = 9\text{V}$ $f = 1\text{ kHz}$		60		dB
V_o	Output voltage with A.L.C. $V_s = 9\text{V}$ $V_i = 100\text{mV}$ $f = 1\text{ kHz}$ $S1 = S2 = S3 = A$		1.1		V
R1	(for SVRF system)	see schematic diagram	7.5		k Ω
R2	(for SVRF system)		120		Ω
e_N	Input noise voltage (for equalization amplifier pin 11) $V_s = 9\text{V}$ $R_g = 4.7\text{ k}\Omega$ $G_V = 40\text{ dB}$ $S1 = B$ $B (-3\text{ dB}) = 22\text{ Hz to }22\text{ KHz}$		1.3		μV
V_{DR}	Drop-out (between pins 14 and 2) $V_s = 9\text{V}$ $I_d = 6\text{ mA}$		0.8		V

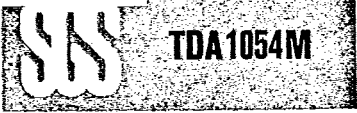


Fig. 1 - Equivalent input spot voltage and noise current vs. bias current (input transistor Q_1)

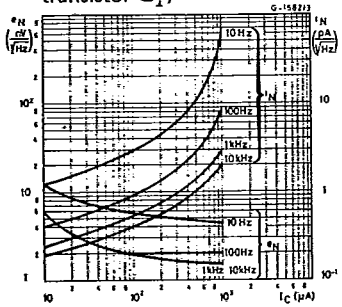


Fig. 2 - Equivalent input noise current vs. frequency (input transistor Q_1)

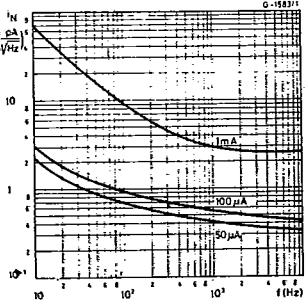


Fig. 3 - Equivalent input noise voltage vs. frequency (input transistor Q_1)

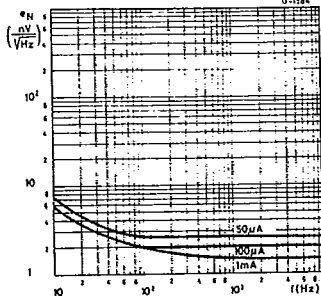


Fig. 4 - Noise figure vs. bias current (input transistor Q_1)

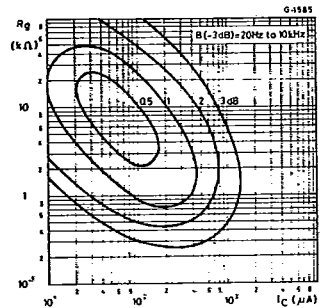


Fig. 5 - Optimum source resistance and minimum NF vs. bias current (input transistor Q_1)

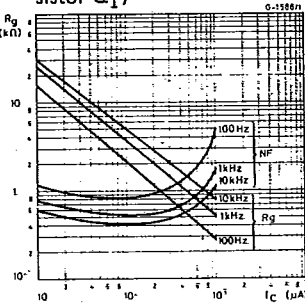


Fig. 6 - Current gain vs. collector current (input transistor Q_1)

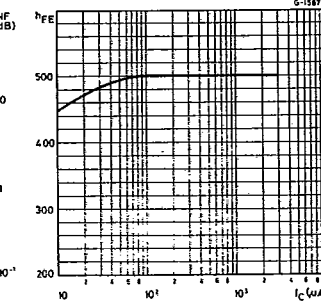


Fig. 7 - Open loop gain vs. frequency (equalization amplifier)

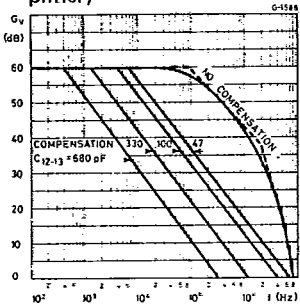
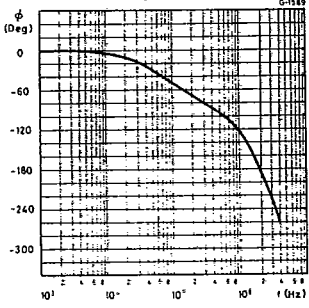
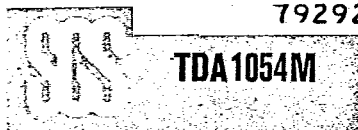


Fig. 8 - Open loop phase response vs. frequency (equalization amplifier)





APPLICATION INFORMATION

Fig. 9 - Application circuit for battery/mains cassette player and recorder

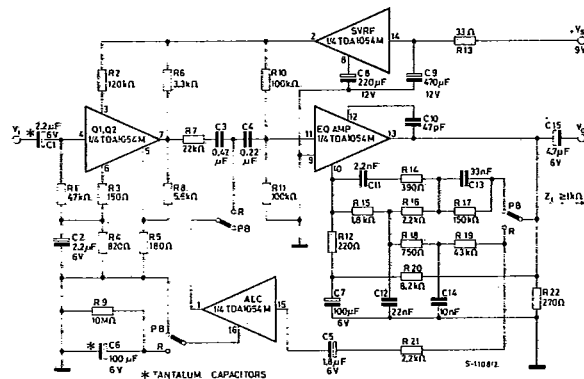
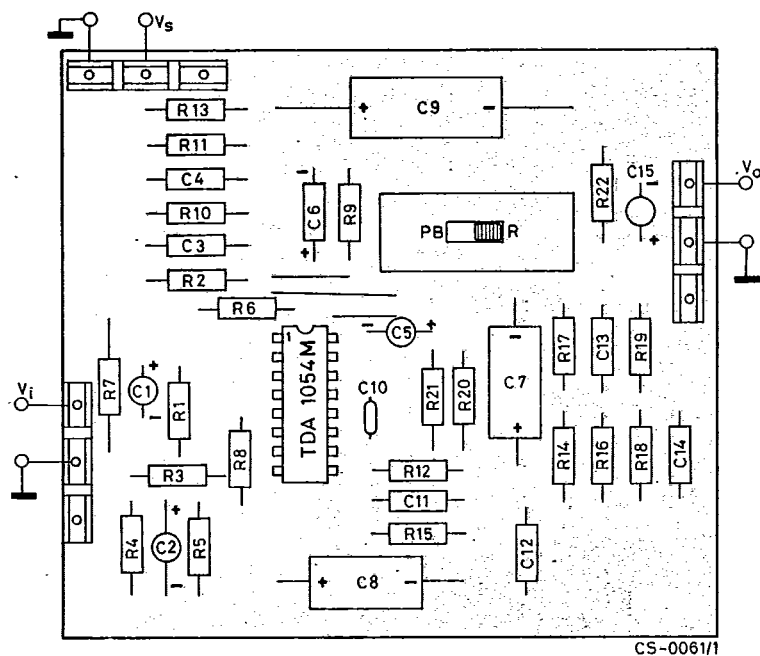


Fig. 10 - P.C. board and component layout for the circuit fig. 9 (1:1 scale)



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TDA1054M

Typical performance of circuit in fig. 9

(T_{amb} = 25°C, V_s = 9V)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
PLAYBACK					
G _v	Voltage gain (open loop)	f = 20 to 20,000 Hz	110		dB
G _v	Voltage gain (closed loop)	f = 1 kHz	57		dB
Z _i	Input impedance	f = 100 Hz f = 1 kHz f = 10 kHz	10 41 43		kΩ kΩ kΩ
Z _o	Output impedance	f = 1 kHz	12	35	Ω
B	Frequency response		see fig. 12		
d	Distortion	V _o = 1V f = 1 kHz	0.1		%
	Output background noise	Z _g = 300 Ω + 120 mH (DIN 45405)	1.3		mV
***	Output weighted background noise		1.3		mV
$\frac{S+N}{N}$	Signal to noise ratio	V _o = 1.3V Z _g = 300 Ω + 120 mH	60		dB
SVR	Supply voltage ripple rejection at the output	f _{ripple} = 100 Hz	30		dB
t _{on} **	Switch-on time	V _o = 1V	500		ms
RECORDING					
G _v	Voltage gain (open loop)	f = 20 to 20,000 Hz	110		dB
G _v	Voltage gain (closed loop)	f = 1 kHz	70		dB
B	Frequency response		see fig. 14		
d*	Distortion without ALC	V _o = 1.1V f = 1 kHz	0.3		%
d	Distortion with ALC	V _o = 1.1V f = 10 kHz	0.4		%
ALC	Automatic level control range (for 3 dB of output voltage variation)	V _i ≤ 40 mV f = 10 kHz	54		dB
V _o	Output voltage before clipping without ALC	f = 1 kHz	2.3		V
V _o	Output voltage with ALC	V _i = 30 mV f = 10 kHz	1.1		V



Typical performance of circuit in fig. 9 (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_l^{**} Limiting time (see fig. 11)	$\Delta V_i = +40 \text{ dB} \quad f = 1 \text{ kHz}$		75		ms
t_{set}^{**} Level setting time (see fig. 11)			300		ms
t_{rec}^{**} Recovery time (see fig. 11)	$\Delta V_i = -40 \text{ dB} \quad f = 1 \text{ kHz}$		150		s
t_{on}^{**} Switch-on time	$V_o = 1.1 \text{ V}$		500		ms
$\frac{S+N}{N}^{****}$ Signal to noise ratio with ALC	$V_o = 1.1 \text{ V} \quad R_g = 470 \Omega$		64		dB

* Measured with selective voltmeter
** This value depends on external network
*** When the DIN 45511 norm for frequency response is not mandatory the equalization peak at 10 kHz can be avoided — so halving the output noise
**** Weighted noise measurement (DIN 45405)

Fig. 11 - Limiting, level setting, recovery time

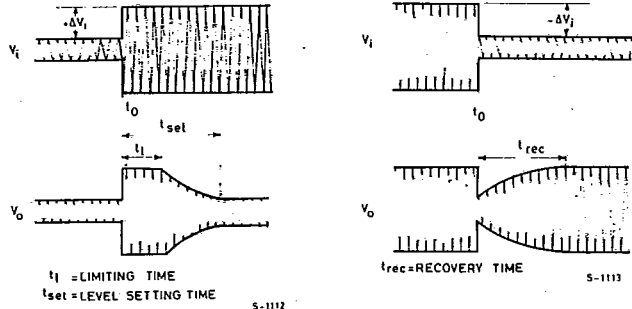


Fig. 12 - Relative frequency response for the circuit in fig. 9 (playback)

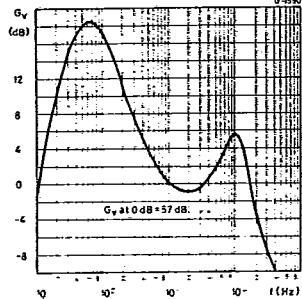


Fig. 13 - Distortion vs. frequency for the circuit in fig. 9 (playback)

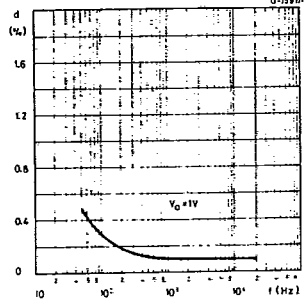


Fig. 14 - Relative frequency response for the circuit in fig. 9 (recording)

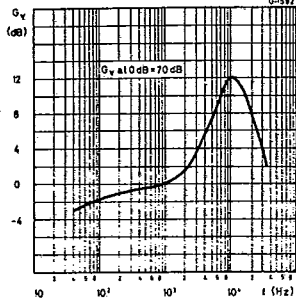
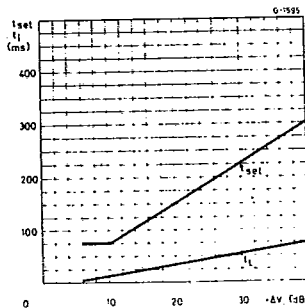


Fig. 17 - Limiting and level setting time vs. input signal variation



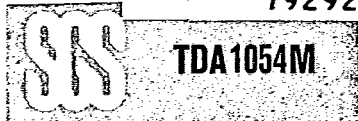
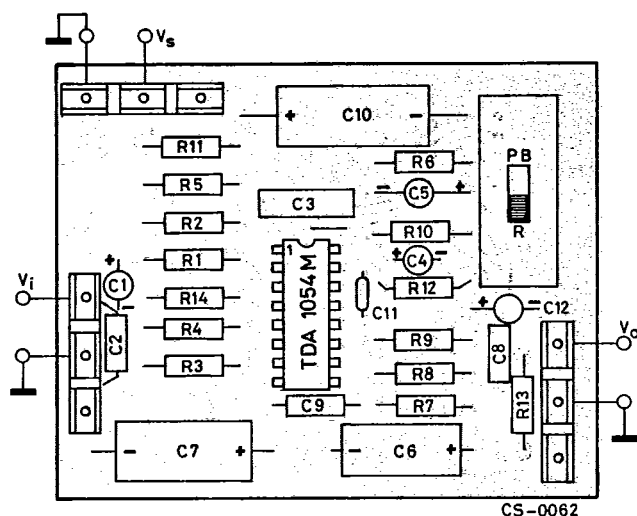


Fig. 19 - P.C. board and component layout for the circuit in fig. 18 (1:1 scale)



Typical performance of circuit in fig. 18
($T_{amb} = 25^{\circ}\text{C}$, $V_s = 9\text{V}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
PLAYBACK					
V_s	Supply voltage	5		12	V
I_d	Quiescent drain current		18		mA
G_v	Voltage gain (closed loop)	$f = 1 \text{ kHz}$	54		dB
B	Frequency response	$f = 100 \text{ Hz}$	12		dB
		$f = 1 \text{ kHz}$	0		dB
		$f = 6 \text{ kHz}$	5		dB
		$f = 10 \text{ kHz}$	11		dB
		$f = 60 \text{ kHz}$	10		dB
d	Distortion	$V_o = 1\text{V}$ $f = 1 \text{ kHz}$	0.6		%
e_N	Output weighted background noise	$Z_0 = 300 \Omega + 120 \text{ mH}$ (DIN 45405)	1.3		mV



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Typical performance of circuit in fig. 18 (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
RECORDING					
G_v	Voltage gain (closed loop)	$f = 1 \text{ kHz}$	70		dB
B	Frequency response	$f = 140 \text{ Hz}$	-3		dB
		$f = 1 \text{ kHz}$	0		dB
		$f = 10 \text{ kHz}$	4		dB
d	Distortion	$V_o = 1.1 \text{ V}$ $f = 10 \text{ kHz}$	0.7		%
ALC	Range for 3 dB of output voltage variation	$V_i \leq 40 \text{ mV}$ $f = 10 \text{ kHz}$	54		dB

Fig. 20 - Complete cassette player and recorder

